Influence of Carbon Capping Materials during High Temperature Annealing on Surface, Defects and Dopant Profile in SiC

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Abstract

This work reports an extensive study on the influence of the capping material being used during high temperature annealing of ion implanted SiC material, on the surface roughness and quality, dopant profile and diffusion, and crystal defects. Chemical vapor deposition (CVD), physical vapor deposition (PVD) and pyrolyzed photoresist (PR) carbon capping materials were investigated in this study. CVD carbon layers, also called Advanced Patterning Film (APF®), were deposited using an Applied Producer®.

INTRODUCTION

During the processing of silicon carbide (SiC) wafers for the fabrication of microelectronics devices such as power MOSFET and diodes [1], a protective layer is deposited on top of the substrate wafer, post ion implantation, to preserve the surface quality by preventing any Si sublimation and step bunching formation as well as the emergence of other surface defects [2, 3, 4], which occur during the high temperature annealing step required for activation of dopants in SiC [5].

This work investigates the influence of the protective capping material being used during such high temperature annealing, on surface and bulk material quality.

EXPERIMENTAL DETAILS

The samples were implanted at high temperature (500 ˚C) with Aluminum ions accelerated at 180 keV and at 2.5E15 ions/cm2 doses in order to realize a peak concentration of about 2E20 ions/cm3 at around 0.2 um deep. The samples were then capped with different carbon-based materials before being annealed for 1800˚C for 30 minutes. The protective cap was then removed by O2 ash with subsequent cleaning and scrubbing, before atomic force microcopy (AFM), surface and bulk photoluminescence (PL) realized on a SICA tool and secondary ion mass spectrometry (SIMS) were performed.

RESULTS

We report an excellent agreement between simulation and post Aluminum implantation profile as shown by SIMS analysis. Additionally, the annealed samples showed very little diffusion as expected, with a minute diffusion towards the surface and a slightly more significant diffusion towards the bulk of the wafer. There is virtually no difference in SIMS profile, either peak concentration amplitude or depth, or total dose, between all wafers capped with different materials (Fig.1).

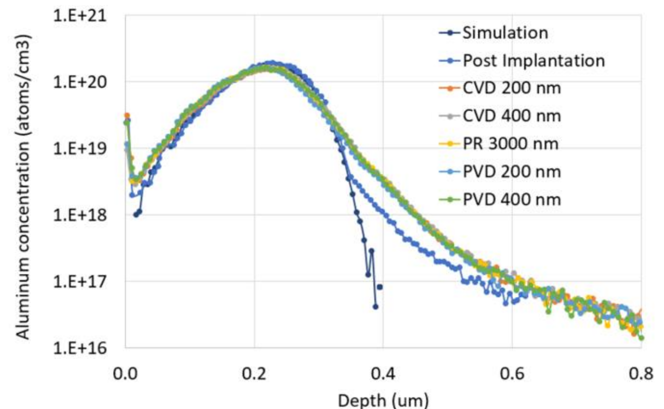

Fig. 1. SIMS results and simulated profiles for post implanted and post annealed with cap removal wafers being implanted with Aluminum ions at 180 keV and 2.5E15 ions/cm2 doses in order to realize a peak concentration of around 2E20 ions/cm3 at about 0.2 um deep.

We also report an unnoticeable change in localized surface roughness (AFM) to moderate increase in global surface roughness (PL) from bare substrate, to implanted wafer while the crystal defect post ion implantation is too severally damaged to show any PL signal. The subsequent annealing step revealed a recovery of the crystallinity and a significant suppression of the damage induced by ion implantation. The lowest AFM measured roughness was observed for PR capped wafers (3000 nm thick) with good uniformity and was comparable with 200 nm thick CVD carbon capped wafer (Fig.2).

The overall surface quality measured on SICA was found to be very similar for all samples with the best quality measured for the 400 nm thick CVD carbon capped wafer and the worst quality measured for the 200 nm thick PVD capped wafer. In terms of crystal defects, all samples show very

similar crystal defect counts around the initial bare wafer value of 18 counts/cm2 with the 400 nm thick PVD carbon capped wafer showing slightly higher defect counts than the other samples at 22 counts/cm2 (Fig.3).

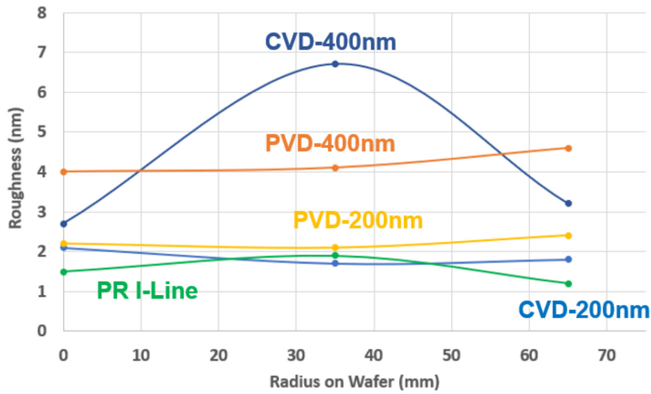

Fig. 2. AFM measurements realized across the capped wafers post implant, annealing and cap removal. 3000 nm thick PR, 200 nm thick CVD, and 200 nm thick PVD capped wafers are showing the lowest AFM roughness with best within wafer uniformity.

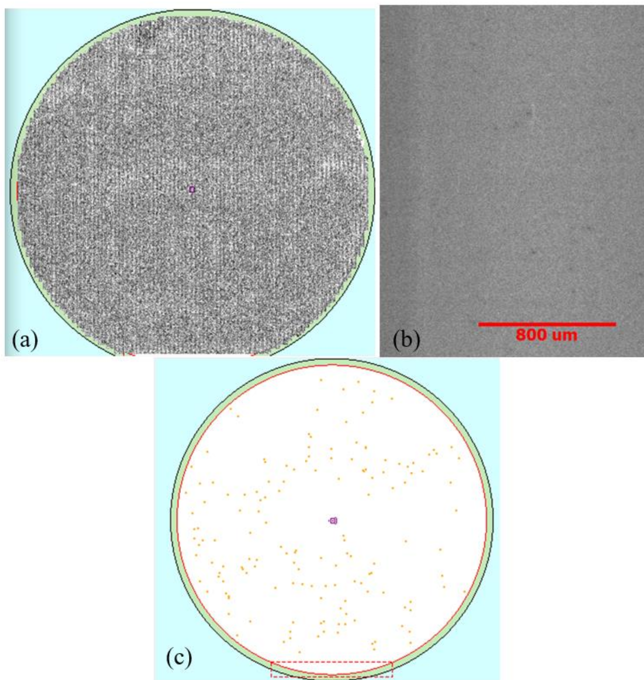

Fig. 3. Example of PL measurements realized on SICA tool, with total surface roughness scanned by DIC at 546 nm confocal microscope (a) and (b), and crystal defects scanned by 313 nm excited PL signal in NIR range with a 10um penetration depth (c).

Conclusion

In conclusion, we report the best overall quality performance for 3000 nm thick PR and 200 nm thick CVD carbon capped wafers. Process throughput consideration should be kept in mind since a graphitization step must be included in the annealing step for PR capped wafer and also outgassing challenges might arise in the furnace. Finally, further work will be needed in assessing the optimal cleaning process for each type of capping material as well as the manufacturing of full test devices for electrical performance comparisons.

TABLE I - Summary of surface and crystal quality measurements performed at center of wafers (C), middle of wafers (M), *i.e.* 4 cm from flat, and edge of wafers (E), *i.e.* 1 cm from flat, using AFM and PL SICA systems.

Cap type	**AFM RMS roughness (nm)**			**PL SICA**	
	C	**M**	**E**	**Global RMS (nm)**	**Crystal defects (cts/cm^2)**
Bare wafer	0.1	0.09	0.1	4.2	19
Implant only	0.1	0.1	0.1	4.7	severe
CVD - 200 nm	2.1	1.7	1.8	4.4	17
CVD - 400 nm	2.7	6.7	3.2	4.3	17
PVD - 200 nm	2.2	2.1	2.4	4.9	17
PVD - 400 nm	4.0	4.1	4.6	4.5	22
PR - 3000 nm	1.5	1.9	1.2	4.5	18

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References

[1] F. Roccaforte, F. Giannazzo and G. Greco, Micro 2, 23–53 (2022)

[2] R. Nipoti, F. Mancarella, F. Moscatelli, R. Rizzoli, S. Zampolli and M. Ferri, Electromechanical and Solid-State Letters, 13 (12) H432-H435 (2010)

[3] M. E. Bathen, M. Linnarson, M. Ghezellou, J. Ul Hassan and L. Vines, Crystals 10, 752 (2020)

[4] K.-K. Choi, J.-Y. Lee, W.-B. Lee, D.-K. Kim and C.-G. Park, J. Nanosci. Nanotechnol. Vol. 18, No. 9 (2018)

[5] M. Spera, D. Corso, S. Di Franco, G. Greco, A. Severino, P. Fiorenza, F. Giannazoo and F. Roccaforte, Mater. Sci. Semicond. Proc. 93, 274-279 (2019).